12. A method of compression for transmission of an encoded digital bit stream having a variable bit rate, comprising the steps of:

detecting a current bit rate of the encoded digital bit stream;

sequentially writing the encoded digital bit stream into a buffer at the detected current bit rate;

reading the encoded digital bit steam out of the buffer at a buffer read bit rate; and,

varying the buffer read bit rate in such a manner as to maintain a substantially constant fullness level of the buffer in response to changes in the detected current bit rate.

13. The method as set forth in Claim 12, wherein the buffer read bit rate is a percentage of the detected current bit rate, which percentage varies inversely in relation to changes in the detected current bit rate.

14. The method as set forth in Claim 12, wherein a delay between the input and output of the buffer varies as a function of the detected current bit rate, so that the delay is relatively higher for a detected current bit rate which is higher than a prescribed bit rate and is relatively lower for a detected current bit rate which is lower than the prescribed bit rate.

REMARKS

Claims 1-9 are pending in the present application. By this Amendment, Applicant has added new Claims 10-14 in order to more positively recite certain aspects of the presently claimed invention. Support for these newly-added claims can be found in the disclosure, including the drawings, as originally filed. Accordingly, Applicant respectfully requests admittance and entry of these newly-added claims.

The instant Office Action rejects Claims 1-2 and 5 under 35 U.S.C. § 102(e) as being anticipated by Balakrishnan (USPN 5,566,208), and rejects Claims 3-4 and 6-9 under 35 U.S.C. § 103 as being unpatentable over Balakrishnan in view of Reininger et al. (USPN 5,426,463). For the reasons explained below, Applicant respectfully traverses these prior art rejections of the pending claims.

Balakrishnan discloses an encoder 48 (see FIG. 3) which includes a compressor 44, an encoder buffer 20, a buffer fullness detector 34, a buffer size controller 50, a quantizer controller 38, and a quantizer 40. The buffer fullness detector 34 detects the fullness level of the encoder buffer 20 and transmits a buffer fullness indication signal indicative of the detected encoder buffer fullness level to the quantizer controller 38. The quantizer controller 38 determines, on the basis of the buffer fullness indication signal, whether the buffer fullness level is greater than a prescribed maximum buffer fullness level or lower than a prescribed minimum buffer fullness level. If the detected buffer fullness level exceeds the prescribed maximum buffer fullness level, then the quantizer controller 38 lowers the quantization step (size) used by the quantizer 40 in encoding the input signal, so that the number of bits utilized for encoding each new unit (e.g., block) of incoming data is decreased, thereby effectively reducing the bit-rate coming from the quantizer 40 into the compressor 44. Conversely, if the detected buffer fullness level falls below the prescribed minimum buffer fullness level, then the quantizer controller 39 increases the quantization step (size) used by the quantizer 40 in encoding the input signal, so that the number of bits utilized for encoding each new unit (e.g., block) of incoming data is increased, thereby effectively increasing the bit-rate coming from the quantizer 40 into the compressor 44. In this manner, the buffer fullness level is maintained within a range between prescribed minimum and maximum buffer fullness levels without violating a constant system time delay constraint, even in the case of variable-rate encoding of the bit stream.

Further, the encoder 48 disclosed by Balakrishnan is a "variable output-rate" encoder, since either the encoder 48 or the communication system 54 can request a transmission rate (output bit-rate) change for encoder 48. In particular, in order to effectuate output bit-rate changes, the buffer size controller 50 receives a request to change the bit-rate from R_{old} to R_{new}. The buffer size controller 50, in response to the bit-rate change request, selectively varies the logical size of the encoder buffer 20 by providing appropriate instructions to the buffer fullness detector 34, e.g., to selectively change the prescribed minimum and/or maximum buffer fullness levels. In this regard, the buffer size controller 50 only changes the system parameters and output bit-rate after determining that such changes will not violate any fixed system constraints, e.g., constant system time delay and physical buffer size. Further, the actual variation of the output-bit rate which is permissible is constrained to a prescribed range which is determined on the basis of the specified values of various system parameters and constraints.

The Balakrishan encoder clearly does not derive a second bit rate (i.e., buffer output bit-rate) as a function of a detected first bit rate of the encoded bit stream, as is required by all of the rejected pending claims of the present application. Rather, the "second bit rate" in the Balakrishan encoder is selected by the encoder 48 or the communication system 54 completely independently of the current bit rate of the input bit stream. As previously mentioned, the actual variation of the output-bit rate which is permissible is constrained to a prescribed range which is determined on the basis of the specified values of various system parameters and constraints. In any event, in response to the output bit-rate being varied within this prescribed range, the buffer size controller 50 selectively changes the logical size of the encoder buffer 20 in accordance with a prescribed algorithm.

In sum, Balakrishan simply does not specify any relationship between the current bit rate

of the input bit stream and the output bit-rate of the encoder buffer 20. Certainly, Balakrishnan does not "derive the second bit rate as a percentage of the first bit rate, which percentage changes inversely in relation to changes in the first bit rate", as is required by the rejected pending claims of the present application. To illustrate this claim limitation more clearly, the following example is given. Namely, assume that the first bit rate is R1 and the second bit rate is R2. The claim limitation "deriving the second bit rate as a percentage of the first bit rate, which percentage changes inversely in relation to changes in the first bit rate" means that R2 = x% R1, and that as R1 increases, x decreases.

As is elaborated upon in the specification of the present application, deriving the second bit rate in the claimed manner results in the maintenance of a substantially constant buffer fullness level. By contrast, Balakrishnan allows the buffer fullness level to vary within a prescribed range which can be varied depending upon the selected output bit-rate, in order to prevent underflow or overflow of the encoder buffer. Clearly, Balakrishnan does not derive the output bit-rate of the encoder buffer (i.e., the "second bit rate") in such a manner as to maintain a substantially constant buffer fullness level. This aspect of the presently claimed invention is more positively recited in newly-added Claims 10-14.

Moreover, deriving the second bit rate in the claimed manner causes the delay between the input and output of the buffer to vary as a function of the detected current bit rate, so that the delay is relatively higher for a detected current bit rate which is higher than a prescribed bit rate and is relatively lower for a detected current bit rate which is lower than the prescribed bit rate. This aspect of the presently claimed invention is more positively recited in newly-added Claim 14. This "tunable delay" feature is certainly not disclosed in the Balakrishnan reference.

Neither Reininger et al., which is applied as a secondary reference in the instant Office

Action, nor any of the other prior art references of record in this case, including the Chujoh and Eyuboglu references cited in the instant Office Action, cure the above-noted deficiencies of the Balakrishnan reference.

Based on the above and foregoing, Applicant respectfully requests withdrawal of the outstanding prior art rejections of Claims 1-9, and further respectfully requests early allowance of Claims 1-9 and newly-added Claims 10-14.

By this Amendment, Applicant has made a sincere effort to place this case in final condition for allowance. However, if it is deemed that there remain any additional issues to be resolved, the Examiner is encouraged to call the Applicant's undersigned representative prior to taking any further formal action in the case. Applicant also hereby petitions and authorizes that any charges that may be necessary to maintain the pendency of this application be charged to Deposit Account No. 14-1270.

Respectfully submitted,

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Date: February 18, 1997

Attorney Docket No.: PHB 33,946